EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	thread with spawn$3 same (pre$1execut$1 near2 thread) same (instruction command)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L2	297	thread with spawn$3 same (instruction command)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L3	6614	718/100-108.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L4	41	L2 and L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L5	16861950	@ad<="19980819"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L6	75	L4 andl5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L7	7	L4 and L5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L8	136601	thread near9 portion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L9	623	L8 near3 execut$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08

EAST Search History

L10	167	L9 with program	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L11	29594611	@py<="2001"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L12	20	L10 and L11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L13	297	thread with spawn$3 same (instruction command)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L14	6614	718/100-108.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L15	41	L13 and L14	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L16	16861950	@ad<="19980819"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L17	75	L15 andl5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L18	136601	thread near9 portion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L19	623	L18 near3 execut$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08

EAST Search History

L20	167	L19 with program	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L21	29594611	@py<="2001"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L22	7	L15 and L16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L23	1	thread with spawn$3 same (pre$1execut$1 near2 thread) same (instruction command)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L24	20	L20 and L21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2007/09/04 11:08
L25	71	(pre$1execut$3 specula$4) near thread same (concurent$2 parallel simultaneous$2)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2007/09/04 11:23
L26	6	(pre$1execut$3 specula$4) near thread same (concurent$2 parallel simultaneous$2) same (cache near miss$2)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2007/09/04 11:26
L27	25	(pre$1execut$3 specula$4) near thread same (concurent$2 parallel simultaneous$2) and (cache near miss$2)	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2007/09/04 11:26
L28	19	l27 not l26	US-PGPUB; USPAT; USOCR; EPO	OR	ON	2007/09/04 11:26

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The **"AND"** operator is unnecessary -- we include all search terms by default. [details]

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D Tullsen
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Speculative Data-Driven Multithreading - all 15 versions »
A Roth, GS Sohi - Proceedings of the Seventh International Symposium on High- ..., 2001 - doi.ieeecomputersociety.org
... a copy of its computation as a new kind of **speculative thread**: a data-driven **thread** (DDT). The DDT executes in **parallel** with the main program **thread**, but ...
Cited by 166 - Related Articles - Web Search

Pointer **cache** assisted prefetching - all 17 versions »
J Collins, S Sair, B Calder, DM Tullsen - Microarchitecture, 2002.(MICRO-35). Proceedings. 35th Annual ..., 2002 - ieeexplore.ieee.org
... **thread** contexts to provide prefetches for a non-**speculative thread**. ... also be accessed in the **near** future and ... and/or pointer **cache**, allowing **parallel** access to ...
Cited by 50 - Related Articles - Web Search - BL Direct

A scalable approach to **thread**-level speculation - all 28 versions »
JG Steffan, CB Colohan, A Zhai, TC Mowry - Proceedings of the 27th annual international symposium on ..., 2000 - portal.acm.org
... build a large-scale **parallel** ma- chine ... Alternatively, the **cache** line could be relinquished ... give exclusiveness to the **speculative thread**, possibly eliminating ...
Cited by 132 - Related Articles - Web Search - BL Direct

Speculative precomputation: long-range prefetching of delinquent loads - all 16 versions »
JD Collins, H Wang, DM Tullsen, C Hughes, YF Lee, ... - ACM SIGARCH Computer Architecture News, 2001 - portal.acm.org
... any two issued bundles are executed in **parallel** without functional ... A p-slice is a **speculative thread** that computes and ... by a delinquent load in the **near** future. ...
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A day in the life of a data **cache** miss - all 7 versions »
T Karkhanis, JE Smith - Workshop on Memory Performance Issues, 2002 - cs.utexas.edu
... reach many hundreds of cycles in the **near** future ... be used for real execution of the main **thread**. ... [13] P. Ranganathan, et al., "Using **Speculative** Retirement and ...
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Dynamic **speculative** precomputation - all 10 versions »
JD Collins, DM Tullsen, H Wang, JP Shen - Proceedings of the 34th annual ACM/IEEE international ..., 2001 - portal.acm.org
... and (3) spawn and manage the execution of **speculative threads**. ... The hardware slice **cache** (shown dashed) is not ... first-serve to static loads which **missed** in L2 ...
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Data speculation support for a chip multiprocessor - all 24 versions »
L Hammond, M Willey, K Olukotun - ACM SIGOPS Operating Systems Review, 1998 - portal.acm.org

... is a technique that enables **parallel** execu- tion ... implementation of the support for **thread**- level speculation ... Our results show that the **speculative** support is ...
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Niagara: a 32-way multithreaded Sparc processor - all 25 versions »
P Kongetira, K Aingaran, K Olukotun - IEEE Micro, 2005 - doi.ieeecomputersociety.org
... The **parallel** execution of many **threads** effectively hides ... However, such a **speculative thread** is assigned a lower ... subsequent t0-add to the **thread**-select stage ...
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Memory latency-tolerance approaches for Itanium processors: out-of-order execution vs. **speculative** ... - all 2 versions »
PH Wang, H Wang, JD Collins, E Grochowski, RM ... - High-Performance Computer Architecture, 2002. Proceedings. ..., 2002 - ieeexplore.ieee.org
... Together the two approaches achieve a **near** addi- tive ... OSC ensures that the **speculative**
thread would neither run ... leave little headroom for the SP **threads** to run ...
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On Dynamic **Speculative Thread** Partitioning and the MEM-Slicing Algorithm - all 12 versions »
L Codrescu, DS Wills - Proceedings of the 1999 International Conference on **Parallel** ..., 1999 - jucs.org
... **Speculative** Data **Cache**, 32Kb,2-way SA, 4 cycle **miss** penalty to ... 4 Partitioning for **thread** speculation. In order to achieve speedup due to **parallel** execution, the ...
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